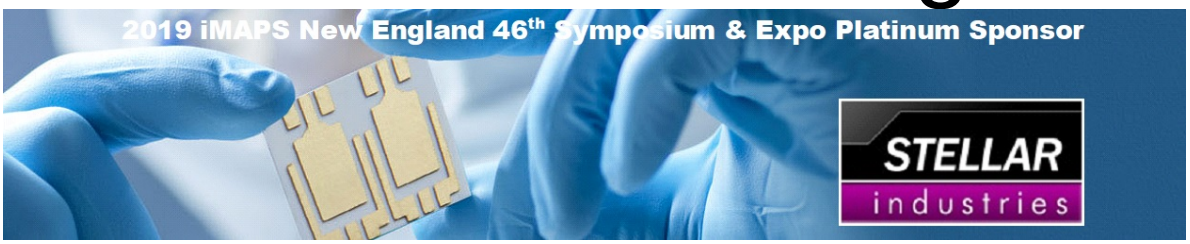
iMAPS New England

46th Symposium & Expo

Technical Program



Tuesday May 7th 2019
Boxboro Regency Hotel
Boxborough, MA

"Connectivity Rocks"

Dmitry Marchenko
IMAPS NE
Chapter President

Lee Levine & Dave Saums
IMAPS NE
Symposium Technical Chairs

iMAPS New England - May 7th, 2019

Welcome to the 46th Annual IMAPS New England Symposium and Expo!

Dear Attendees, Exhibitors, Presenters and Organizers!

This event is a highlight of the yearly activity of our Chapter, aimed to bring to you an opportunity to network with your peers and gain an insight into trends moving electronics packaging industries in our region. Our volunteers prepared an extensive one-day Technical Program packed with latest developments in copper pillars, advanced dielectrics, high power laser diodes, quantum dot applications, GaN for 5G, MEMs energy harvesting, silver sintering and 3D printable additive manufacturing.

This is a second time in a row our Technical Symposium Co-Chairs Lee Levine and Dave Saums, together with Sessions Chairs assembled presentations for a very strong Technical program. How do they do it? Join our Executive Committee and you will find out! We are currently looking for energetic contributors for several key Committee roles.

Our 46th Symposium theme, “Connectivity Rocks” was suggested by one of our active members, we are stepping up our efforts to engage a wider audience and build our events based on your feedback. You probably have noticed a pickup in communications from our Publicity Chair Harvey Smith, looking for membership input.

The Sponsorship program plays a huge part in feasibility and quality of our event, please take your time to recognize the companies that year after year support our Symposium as an exchange of ideas and knowledge – our Gold Sponsors MRSI, Geib Refining Corp, TJ Green Associates, RIV, Centerline Technologies, Mini-Systems Inc, LFG Micro, TenTech LLC, PEI, Accumet / Laser Services, Innovative Fabrication, Adtech Ceramics. I would like to personally thank STELLAR for becoming the first Platinum Sponsor of our Symposium.

The Expo was sold out several months prior to the event thanks to fantastic effort of our Exhibits Chair Michael Toro. Michael and other members of the Executive Committee – Matt, Jeremy, Harvey, Jon, John B, Joe, Tom, Dipak, Amaresh, John R, Jim M - worked very hard this year to produce the event worthy of its fame. Special thanks to Judi Eicher for working out logistical issues and delivering creative arrangement ideas. Quite an impressive track record for an all-volunteer regional chapter committee, don’t you think?

After the first half of our Technical Program we will be waiting for you in the Exhibit Hall for Luncheon and Keynote presentation. It’s a perfect opportunity to network with other attendees and prospective suppliers. Post Technical Program conclusion I hope to see you back in the Exhibit Hall for refreshments, entertainment and prize raffles.

Thank you for choosing to attend our Symposium, I hope you will find it a highly valuable experience!

Dmitry Marchenko

Dmitry Marchenko

President, iMAPS New England Chapter

Symposium Technical Chairs' Welcome Letter

Lee Levine

We would like to welcome everyone to the 46th Annual New England *i*MAPS Symposium. Thanks to all the Session Chairs, we've compiled an engaging program of technical talks on many of today's hot topics that will peak the interest of every attendee. We hope you take full advantage of the opportunity to interact with the speakers and each other in a learning environment that is only available at this unique one-day symposium. Below is a brief summary to help you on your way and don't forget to spend time in the exhibit hall, because after all, without the support of the exhibitors, this day wouldn't be possible.

Dave Saums

Advanced Electronics: Copper pillars, adhesive bonding, advanced dielectrics, fan-out wafer level packaging, cost-reducing production volume testing and thermal stability maps will all be included topics in the advanced packaging session.

Photonics and Optoelectronics Packaging: Holographic vibrometry for MEMS, Die bonding high-power laser diodes (HPLD), the IOT (internet of things) for industrial automation sensors, Quantum dots in long wavelength applications and new packaging strategies for integrated photonics are featured topics in the Optoelectronics session.

RF and Microwave - Innovations and Emerging Technologies: There will be two RF sessions, morning and afternoon. In the morning there will be two talks on GaN on Silicon for 5G applications, GaN Amplifiers for MMICs, TPG (graphite) for thermal management, and recent developments in capacitors.

In the afternoon session, we will have presentations on the effects of high temperatures on LTCC dielectrics, thermoplastic polyimide (TPI) adhesives for RF, epoxy preforms for RF, and the hermetic sealing of metal packages.

Novel Packaging: New packaging for medical implants, organic packaging for applications with liquid exposure, medical imaging applications, a MEMS-based energy harvester, and commercial challenges for medical MEMS applications are all included in the Novel Packaging session.

Interconnects: High-reliability copper alloy bonding wire, a review of MIL-STD-883 visual inspection criteria, sintered silver die attach material, zero outgassing and residue underfill, and the use of Design of Experiments (DOEs) for understanding complex processes will be presented in this Interconnects session.

Printed Electronics: Phase shifters, photonic curing, tunable inks, testing and analysis of printed conductive inks, and 3-D printable additive manufacturing will all be topics in the printed electronics session.

Interactive Dialogue Session: This session format was introduced in 2018 and was exceedingly successful, as all presenters found that the format allowed for in-depth discussion, one-on-one and in groups, around each set of poster material. We will again have both industry and academic presentations on key selected topic, where each author will have a two-hour time period in which to answer questions and discuss the research topic and methodologies employed, for topics including research, manufacturing process development, and product applications.

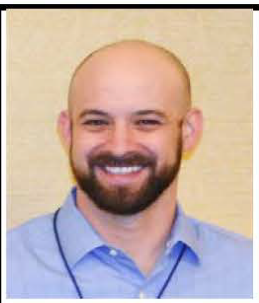
Kind Regards,

Lee Levine Dave Saums

2019 *i*MAPS New England Symposium Technical Chairs

IMAPS New England Executive Committee 2018-2019

Dmitry Marchenko
President
BAE Systems



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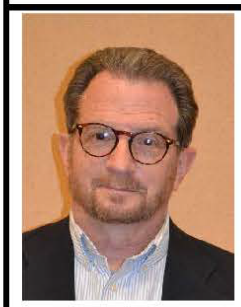

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John Redman *
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Keynote Lunch Address

"General Applications of AESA Radar Technology"

Presented by Gerald (Jerry) Charlwood

Director, Lightwave Antenna Business Unit

– MACOM –

Email: jerry.charlwood@macom.com

11:50 AM – Exhibit Hall

Keynote Abstract:

In order to provide affordable radar systems that are capable of performing multi-function operations in harsh environments Active Electronically Steered Array approaches are required to meet today's missions from Air Traffic Control to Air Defense. The flexibility of the AESA Tile based approach to radar implementation supports a wide range of applications. Active Antenna technologies from MACOM are providing an affordable approach to supporting these applications (Air Traffic Control, Weather tracking, Air Defense, Counter UAS). Specific applications for the future out to 2025 will be the focus of the discussion.

Biography:

Jerry has 33+ years of leadership in Systems Engineering, Program Management, Engineering Management, and Business Development/Capture Management related to sensor and weapons programs for Navy, Army, Missile Defense and Marine Corps programs including AESA radar, communications, ESM systems, navigation products, combat systems, ship and vehicle integration. Jerry is currently the Business Unit Director at MACOM developing AESA tiles for radar applications.

46th Annual Symposium - Tuesday May 7th, 2019

Technical Program - Quick Guide

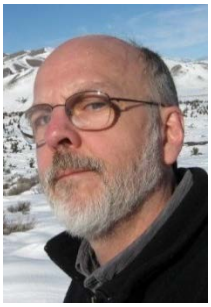
Session			Room	Chairs	# Papers
Sessions 8:30 – 11:30 AM					
Morning	A:	Advanced Packaging	Colonial	Frank Muscolino Richard Hollman	5
	B:	Printed Electronics	Cotillion	Mary Herndon Jim King	5
	C:	RF and Microwave – 5G Innovations & Microwave Emerging Technologies I	Seminar	Tom Terlizzi Chandra Gupta	5
	D:	Interconnects	Directors	Lee Levine William Boyce	5
	E:	Interactive Posters (all day)	Exhibit Hall Presenters: 2:00 – 4:00 PM	Dipak Sengupta Michael Johnson Dave Saums	18
Lunch Break – Exhibit Hall – 11:30AM – 1:00PM					

Sessions 1:00 – 3:30 PM					
Afternoon	F:	Novel Packaging Applications	Colonial	Jim Ohneck Richard Elbert	5
	G:	Photonics & Optoelectronics Packaging	Cotillion	Yi Qian Jin Li	5
	H:	RF and Microwave – 5G Innovations & Microwave Emerging Technologies II	Seminar	Stephen Bart Rick Morrison	4

Exhibit Hall Open 9:00AM – 4:30PM

46th Annual Symposium - Tuesday May 7th 2019

Morning Technical Program – Session Chairs

Session		Chair		Chair	
A:	**Advanced Packaging**	**Frank Muscolino** **President** **Advanced Assembly Technologies** 781-883-5428 Frank@advancedassemblytechnologies.com		**Richard Hollman** **Principal Process Engineer** **ASM Pacific Technology** 978-436-2393 richard.hollman@asmpt.com	
B:	**Printed Electronics**	**Mary Herndon** **Engineering Fellow** **Raytheon IDC** 978-726-6394 Mary_K_Herndon@raytheon.com		**Jim G. King** **President** **King Technologies** 978-456-8040 jjjking@att.net	
C:	**RF and Microwave – 5G Innovations & Microwave Emerging Technologies I**	**Tom Terlizzi** **Vice President** **GM Systems LLC** 631-269-3820 terlizzi@gmsystems.com		**Chandra Gupta** **Communications & Power Industries, LLC** 516-807-9488 c.gupta@ieee.org	
D:	**Interconnects**	**Lee Levine** **Principal Consultant** **Process Solutions Consulting** 610-285-6367 levilr@ptd.net		**Bill Boyce** **Packaging & Process Engr.** **WBoyce Consulting** 401-523-6465 williamboyce76@gmail.com	

46th Annual Symposium - Tuesday May 7th 2019
Interactive Dialog Poster Program – Session Chairs

E:	 **Dipak Sengupta** **Consultant** **Analog Devices Inc., Ret.** 978-270-1923 sngdsg@gmail.com	 **Michael Johnson** **Principal Mfg. Engr.** **MACOM** 978- 656-2842 michael.johnson@macom.com	 **Dave Saums** **Principal** **DS&A LLC** 978 479 7474 dsaums@dsa-thermal.com

Afternoon Technical Program – Session Chairs

Session		Chair		Chair	
F:	**Novel Packaging Applications**	**Jim Ohneck** **CEO** **Laser Therapy Services** 440-785-2298 johneck@lasertherapyservices.com		**Rick Elbert** **Field Application Engineer** **Cicor Group** 330-813-1933 Richard.Elbert@cicor.com	
G:	**Photonics & Optoelectronics Packaging**	**Yi Qian** **VP of Marketing** **MRSI Systems** 978-495-9742 yi.qian@mrsisystems.com		**Jin Li** **Sr. Product Mgr.** **Cambridge Technology** 781-266-5217 Jin.Li@cambridgetechnology.com	
H:	**RF and Microwave – 5G Innovations & Microwave Emerging Technologies II**	**Stephen Bart** **Dir. Environmental Sensing** **InvenSense SSBC** 857-268-4361 sbart@invensense.com		**Rick Morrison** **Engineering Mgr.** **Draper** 617-258-3420 rmorrison@draper.com	

Special Feature... at The 46th Symposium & Expo

"Redefining Electro-Thermal Simulation for the Electronics Industry"

Presenter: Priam Fernandes

A Technical Workshop

10th ANNIVERSARY 6SigmaET by Future Facilities

Sponsored By Future Facilities - 1:00 to 3:00 pm

This workshop will cover multiple examples from chip, board and system level design as well as electro-thermal co-simulation. The traditional approach to electronics thermal simulation has not kept pace with current technology. Users of traditional software are still facing the same obstacles: usability, managing CAD data/model complexity and prohibitive solution times.

Fortunately, there is an alternative. 6SigmaET is the new standard for electronics thermal CFD. ET has redefined expectations for model size (100M+ cells), CAD interoperability (no simplification required), scalability (cluster solve) and meshing (push button, rules driven).

All Particiants will receive a complimentary 30-day trial of the software and a special incentive for purchase at the end of the evaluation.

All 46th Symposium & Expo Attendees May Participate - Regardless of Registration Type..!

Morning Session	Colonial Room
8:30 – 11:05	**Session A: Advanced Packaging** **Frank Muscolino & Richard Hollman – Co-Chairs**
8:30	**"Thermodynamic Stability MAPS: A Powerful Engineering Design Tool", Robert H. Lacombe -** Materials Science and Technology Conferences, LLC, Hopewell Junction, NY
8:55	**"Void-Free Copper Pillar Hybrid Bonding Using a Polymer Adhesive and Chemical Mechanical Polishing", Hua Dong** – DowDuPont Specialty Products (DuPont) Division, Marlborough, MA
9:20	**"Adhesion Considerations in Designing Dielectric Materials for Advanced Packaging Applications", Michaela Connell,** Stephanie Dilocker, Ognian Dimov, Sanjay Malik - Fujifilm Electronic Materials, Inc, North Kingstown, RI
9:45 – 10:15	**Coffee Break in the Exhibit Hall**
10:15	**"Volume Production Testing of Silicon Photonics Modules Case Study: Wafer Sort Test Coverage versus Through-Put", John Ritchie** - Straits Hi-Rel Pte. Ltd. Singapore
10:40	**"An Electrical Fan-Out Wafer Level Packaging Test Vehicle and Update on the Advanced System Integration Program", John Allgair PhD** , Amit Kumar, and Ankineedu Velaga – BRIDG, NeoCity, FL
11:30 – 1:00	**Lunch & Keynote in the Exhibit Hall**

Afternoon Session	Colonial Room
1:00 – 3:05	**Session F: Novel Packaging Applications** **Jim Ohneck & Richard Elbert – Co-Chairs**
1:00	**"Medical Imaging Applications - the Underlining Technology", Dan Negrea** – AEMtec GmbH, Berlin, Germany
1:25	**"Fully Organic Packaging for Applications with Liquid Exposure", Susan Bagen -** Micro Systems Technologies, Inc., Lake Oswego, NY; Eckardt Bihler, Marc Hauer - MST Dyconex AG, Bassersdorf, Switzerland
1:50	**"Advancement in Microelectronic Packaging for Medical Implants", Caroline K. Bjune** - Draper Laboratory, Cambridge, MA
2:15	**"Think Like an Innovator, Act Like an Entrepreneur", Angelique Johnson,** MEMStim LLC, Louisville, KY
2:40	**"Fabrication and Packaging of a MEMS Based Energy Harvester", Yuechen Yang,** Ujwal Radhakrishna, Dennis Ward, Anantha P. Chandrakasan, Jeffrey H. Lang - MIT, Cambridge, MA
3:00 – 4:30	**Refreshments, Awards, & Raffles in the Exhibit Hall**

Morning Session	Cotillion Room
8:30 – 11:05	**Session B: Printed Electronics** **Mary Herndon & Jim G. King – Co-Chairs**
8:30	**"Curing Printed Conductive Layers on Low-Temperature Substrates with Intense Pulsed Light", Guinevere Strack,** Andrew Luce, Craig Armiento, and Alkim Akyurtlu - Electrical and Computer Engineering Department, Printed Electronics Research Collaborative, UMass Lowell, Lowell, MA
8:55	**"Testing Methodology and Analysis of Fusing Current of Printed Conductive Inks on Dielectric Substrates", Elicia K. Harper**, Emily K. Engel, Susan C. Trulli, and Kara P. Upton - Raytheon Integrated Defense Systems, Andover, MA
9:20	**"Barium Strontium Titanate Nanocomposite Dielectric Inks for Flexible RF and Microwave Electronics Applications", Oshadha K Ranasingha,** Mahdi Haghzadeh, Craig Armiento, and Alkim Akyurtlu - Electrical and Computer Engineering Department, Printed Electronics Research Collaborative, Raytheon – UMass Lowell, Lowell, MA
9:45 – 10:15	**Coffee Break in the Exhibit Hall**
10:15	**"Printed Phase Shifters for Antenna Arrays", Shokat Ganjeheizadeh Rohani,** Mahdi Haghzadeh, Craig Armiento, and Alkim Akyurtlu, Electrical and Computer Engineering Department, Printed Electronics Research Collaborative, Raytheon – UMass Lowell, Lowell, MA
10:40	**"Novel Techniques for Additive Manufacturing of Functional Materials", L. Parameswaran**, , R. Mathews, L.M. Racz, Duncan, M. Plaut, T. Fedynyshyn - MIT Lincoln Laboratory, Lexington, MA; Y. Kornbluth, L.F. Velásquez-García, Massachusetts Institute of Technology, Cambridge, MA; B. S. Uzel, R. Weeks, and J.A. Lewis - Harvard, Cambridge, MA
11:30 – 1:00	**Lunch & Keynote in the Exhibit Hall**

Afternoon Session	Cotillion Room
1:00 – 3:05	**Session G: Photonics & Optoelectronics Packaging** **Yi Qian & Jin Li – Co-Chairs**
1:00	**"The Evolving Face of Integrated Photonics: New Packaging Strategies", Juejun Hu,** Shaoliang Yu, Haijie Zuo, Jerome Michon, Derek Kita, Sarah Geiger, Qingyang Du, and Tian Gu – MIT, Cambridge, MA
1:25	**"Quantum Dots in Long Wavelength Applications", Xifeng Qian**, Elif Demirbus - UMass Lowell, Lowell, MA
1:50	**"Full-field Digital Holographic Vibrometry for Characterization of Optoelectronic Packaging and MEMS", Cosme Furlong,** Payam Razavi, Morteza Khaleghi, and Ivo Dobrev - Center for Holographic Studies and Laser micro-mechaTronics (CHSLT), Mechanical Engineering Department, Worcester Polytechnic Institute, Worcester, MA
2:15	**"Industrial Automation Sensors and Industrial Internet of Things (IIOT)", Yongyao Cai** - Rockwell Automation, Chelmsford, MA
2:40	**"High-Speed, High-Precision and High-Flexibility, Automated Die-Bonder for High-Power Laser Diode (HPLD) Packaging", Rajiv Pandey**, Jason Liu, Julius Ortega, – MRSI Systems, N. Billerica, MA
3:00 – 4:30	**Refreshments, Awards, & Raffles in the Exhibit Hall**

Morning Session	Seminar Room
8:30 – 11:05	**Session C: RF and Microwave – 5G Innovations & Microwave Emerging Technologies I** **Tom Terlizzi & Chandra Gupta – Co-Chairs**
8:30	"**100nm GaN on Si Technology for 5G Applications**", **Charles Edoua,** OMMIC, Limeil-Brévannes Cedex France
8:55	**"A Reconfigurable S/X-Band 25W GaN Power Amplifier MMIC", Charles F. Campbell**, Kevin W. Kobayashi and Cathy C. Lee - Qorvo Infrastructure and Defense Products, Richardson, TX
9:20	**"GaN-on-Silicon for 5G Radios", Timothy Boles** – MACOM Technology Solutions
9:45 - 10:15	**Coffee Break in the Exhibit Hall**
10:15	**"Advancement in TPG Graphite Based Technology for Chip-level Thermal Management", Wei Fan,** Liu Xiang, Brian Kozak, Kristi Scherler, and Greg Shaffer – Momentive Performance Materials, Inc., Strongsville, OH; Garry Wexler – Henkel Corporation, Prescott, WI
10:40	**"Think Outside The Cylinder", Richard Howell -** Cornell Dubilier / TTI, Inc., Boston, MA
11:30 – 1:00	**Lunch & Keynote in the Exhibit Hall**

Afternoon Session	Seminar Room
1:00 – 2:40	**Session H: RF and Microwave – 5G Innovations & Microwave Emerging Technologies II** **Stephen Bart & Rick Morrison – Co-Chairs**
1:00	**"Epoxy Preform Guidelines for RF Microwave Module Assembly", Scott MacKenzie**, President - Bonding Source, Manchester NH
1:25	**"Thermoplastic Polyimide (TPI) Adhesive Technology for RF Circuit", Jim Fraivillig,** Fraivillig Technologies, Boston, MA
1:50	**"Elevated Temperature Impact on Performance of LTCC Dielectrics", Anton Polotai,** Jim Henry, David Thoss, Yi Yang, and Sanjay Chitale - Ferro Corporation, Independence, OH
2:15	**"Reliable Sealing of Metal Packages", Tom Salzer** – Hermetric, Inc., Bedford, MA
3:00 – 4:30	**Refreshments, Awards, & Raffles in the Exhibit Hall**

Morning Session	Directors Room
8:30 – 11:05	**Session D: Interconnect** **Lee Levine & William Boyce – Co-Chairs**
8:30	**"The Use of Designed Experiments in Process Development", Lee Levine -** Process Solutions Consulting, Inc., New Tripoli, PA
8:55	**"Zero Outgassing and Flux Residue Compatible Underfill", John Yin,** Mary Liu and Wusheng Yin, PhD - YINCAE Advanced Materials, LLC, Albany, NY
9:20	**"Introduction of Die Attach Hybrid Silver Adhesive Technology", Koyo Kobori –** Tanaka, Kikinzoku Kogyo, Japan
9:45 - 10:15	**Coffee Break in the Exhibit Hall**
10:15	**"A Critical Review of MIL-STD-883 Wirebond Visual Inspection Criteria", Thomas Green -** TJ Green Associates LLC, Bethlehem PA
10:40	**"Introduction of Copper Alloy Bonding Wire for the High Rel Industry", William Crockett Jr. –** Tanaka, Japan
11:30 – 1:00	**Lunch & Keynote in the Exhibit Hall**

Exhibit Hall

Session E: Interactive Poster Session - Viewing All Day

Dipak Sengupta, Michael Johnson, & Dave Saums – Co-Chairs

Interactive Discussion Period: 2:00 PM – 4:00 PM

"Challenges in Solder Attaching an Air Cavity Device Using Tin Bismuth Solder", Michael Johnson - MACOM Technology Solutions, Lowell, MA

"Advanced Thermal and Embedded Solutions for Laminate Substrate Designs", Abimael Reyes, Eric Eilenberg, and Paul Hogan **-** MACOM Technology Solutions, Lowell, MA

"Evaluation of the Thermal Performance of a Light Emitting Diode (LED) Package Manufactured Using POL-kW Packaging Technology", Anisha Walwaikar[1], Christopher Kapusta[2], Liang Yin[2], Kaustubh Nagarkar[3], Krishnaswami Srihari[1], Daryl Santos[1] - [1]Department of Systems Science and Industrial Engineering, SUNY Binghamton, NY; [2]GE Global Research Center, Niskayuna, NY; [3]GE Ventures, Niskayuna, NY

"Transient Liquid Phase Bonding Technology of Bi-Ni System for High-Temperature Electronics", Hamid Fallahdoost and Junghyun Cho - Materials Science & Engineering Program, SUNY Binghamton Binghamton, NY

"Evaluation of Mechanical Properties and Adhesion of Various Conformal Coatings Used in Electronic Packaging", Preeth Sivakumar and Junghyun Cho - Department of Mechanical Engineering, SUNY Binghamton, Binghamton, NY

"The Effect of Solder Paste Volume on Surface Mount Assembly Self-Alignment", Pan[1], J. H. Ha[1], H.Y. Wang[1], I. Parviziomran[2], D.H. Won[2], S.B. Park[1] -[1] Mechanical Engineering, SUNY Binghamton, NY; Systems Science and Industrial Engineering, SUNY Binghamton, NY; [2]Koh Young Technology Inc., Seoul, Korean.

"A Study Of Substrate Models And Its Effect On Package Warpage Prediction", Van-Lai Pham, Huayan Wang, Jiefeng Xu, Charandeep Singh, Jing Wang, & Seungbae Park - Department of Mechanical Engineering, SUNY Binghamton, Binghamton, NY

"Time 0 Void Evolution And Effect On Electromigration", Jiefeng Xu[1], Scott McCann[2], Huayan Wang[1], VanLai Pham[1], Stephen R. Cain[1], Gamal Refai-Ahmed[2], S.B. Park[1] - 1 Department of Mechanical Engineering SUNY Binghamton, Binghamton, NY; 2 Xilinx, Inc., San Jose CA

"Characterization of Silicon Die Filleting Process through Dispensing", Ludovico Cestarollo, Mohammed Alhendi, Darshana Weerawarne & Mark Poliks – SUNY Binghamton, Binghamton, NY

"Process and Reliability Investigation of Sn-Bi Assembly for BGA Components", Chongyang Cai, Jiefeng Xu, Huayan Wang, Seungbae Park - Department of Mechanical Engineering, SUNY Binghamton, Binghamton, NY

"Product Level Design Optimization for 2.5D Package Shock Impact Reliability", Huayan Wang[1], Jing Wang[1], Jiefeng Xu[1], Vanlai P ham[1], Seungbae Park[1,] Hohyung Lee[2], Gamal Refai-Ahmed[2] -[1]SUNY Binghamton, Binghamton, NY; [2]Xilinx Inc, San Jose, CA

"Testing and Evaluating Flexural Strength of Stacked Silicon Die Configurations", Ankita Korad[(1)], Daryl Santos[(1)], Krishnaswami Srihari[(1)], Salvatore Napoli[(2)] – [1]Watson Institute for Systems Excellence, SUNY Binghamton, Binghamton, NY; [2] Analog Devices, Inc., Wilmington, MA

"A High Spatial Resolution Measurement of Trap States and Charge Motion in Non-Traditional Semiconductors", Jason P. Moscatello[1], Christina L. McGahan[2], Katherine E. Aidala[3,] [1]Researcher, Department of Physics, Mount Holyoke College[2]Post-doctoral Researcher, Department of Physics, Mount Holyoke College,[3]Chair of Physics, Professor of Physics, Chair of Engineering, Mount Holyoke College

"Liquid Metal Innovations for High-Performance TIMs", Timothy Jensen - Senior Product Manager

Solder Preforms & Thermal Technologies, Indium Corporation, Clinton, NY

"Advances in Thermal Management", Brian Bruce, Mavyn Holman, & Paul Huynh – Epoxy Technology, Billerica, MA

"Design of a Thermal Interface Material Cycling Reliability Test Program for Semiconductor Test", David L. Saums*, Principal - DS&A LLC, Amesbury MA; Tim Jensen, Sr. Product Manager - Indium Corporation, Clinton NY; Ron Hunadi, Market Development Manager - Indium Corporation, Clinton NY; Mohamad Abo Ras, CEO and Co-Founder - Berliner Nanotest und Design GmbH, Berlin, Germany

"FTIR Based Identification Method of Underfill Materials and Matching System", Junbo Yang, Seungbae Park – SUNY Binghamton, Binghamton, NY

"The Effect of Solder Paste Volume on Chip Resistor Solder Joint Fatigue Life", Huayan Wang, Ke Pan, Jonghwan Ha, Chongyang Cai, Jiefeng Xu, Seungbae Park – SUNY Binghamton, Binghamton, NY

Morning Technical Program

Session A: Advanced Packaging

Chaired by Frank Muscolino (Adv. Assembly Tech.) & Richard Hollman (ASM Pacific Tech.)
Colonial Room - 8:30 AM – 11:05 AM

8:30 – 8:55 AM Colonial Room

"Thermodynamic Stability MAPS: A Powerful Engineering Design Tool", Robert H. Lacombe - Materials Science and Technology Conferences, LLC, Hopewell Junction, NY

The first phase of a typical plan for an innovative device or advanced structure start with a paper outline of what is to be achieved and how it will surpass the current technology. At this stage all looks well and eminently doable. However, advanced and innovative structures typically involve newer material sets or as yet unproven applications of current materials and this is where problems tend to arise. Introducing different materials into an existing structure tends to introduce as yet unforeseen material incompatibilities which can lead to delaminations, fracture or a host of other problems.

One method for overcoming these obstacles is through the use of thermodynamic stability maps which are generated through a process of materials characterization and computer modeling. The stability map can be thought of as a guide through the minefield of materials related thermodynamic instabilities that can derail development programs, cause interruptions in manufacturing or in a worse case give rise to delayed failure after product has shipped.

The stability map idea leads to the concept of "Engineering Design for Unconditional Structural Stability in Regard to All Anticipated Loading Conditions". A detailed example will be given for the case of soldering pins onto a large multichip module where the failure of even one pin could destroy the modules functionality and the module was too expensive to simply discard.

8:55 – 9:20 AM Colonial Room

"Void-Free Copper Pillar Hybrid Bonding Using a Polymer Adhesive and Chemical Mechanical Polishing", Hua Dong – DowDuPont Specialty Products (DuPont) Division, Marlborough, MA 01752

To maintain the industry goal of increasing performance with every new generation of technology, it is necessary to further shrink the package size in the z-dimension through the use of 3D-TSV and copper pillar structures. Previously, Niklaus et al[1] and McMahon et al[2] demonstrated the ability to bond copper-polymer structures using a copper dual damascene integration scheme. In this approach, copper slurries removed the copper overburden and, although bonding of the copper areas was achieved, gaps between the polymeric adhesive layers were visible after bonding. To overcome this issue, we have developed two approaches to planarize both the copper pillar as well as the polymeric adhesive. The first approach relies on non-selective CMP of the two materials; the second approach relies on sequential steps of polymer and copper removal.

Planarization studies were performed on a commercial tool using experimental slurries that were tuned to be non-selective and have similar removal rates for both copper and polymer, or to be selective and remove only one of the materials. By optimizing the polishing process conditions, we were able to achieve selectivity as low as 1.6:1 for the non-selective slurries and as high as 1000:1 for the selective slurries on blanket wafers. Once optimized, the goal of the CMP process will be to completely remove the polymer from the top of the pillar and planarize the copper pillars while leaving them protruding by less than ~100 nm above the surface of the polymeric adhesive.

Currently, we are performing chip-to-chip bonding trials of partially cured polymeric adhesive after various CMP methods. In addition, copper to copper hybrid bonding using singulated dies with a commercial flip chip bonding tool are also in progress to demonstrate the electrical continuity and void free bonding. Preliminary reliability studies will start once the bonding process is fully optimized.

[1] F. Niklaus et al, Journal of the Electrochemical Society, 2006, 153, G291.
[2] McMahon et al, IEEE Electronic Components and Technology Conference, 2008, 871.

9:20 – 9:45 AM Colonial Room

"Adhesion Considerations in Designing Dielectric Materials for Advanced Packaging Applications", Michaela Connell, Stephanie Dilocker, Ognian Dimov, Sanjay Malik - Fujifilm Electronic Materials, Inc, North Kingstown, RI
Advanced packaging relies more and more on multilayer RDL stacking. In the complex integration schemes employed in advanced package integration, organic dielectric materials are expected to be in contact with a plurality of heterogeneous materials like copper, epoxy molded compound (EMC), nitride, oxide, aluminum and a variety of other low-k films. Copper traces are either embedded into organic dielectric material as in a typical Damascene scheme or are deposited on top of dielectric film in a typical SAP scheme. There are additional steps such as under bump

metallization, grinding to planarize topography or expose chip surface, solder balling, under-filling and die-attach where dielectric film is subjected to harsh thermal, chemical and mechanical stresses.

Complexity in design and architecture of advanced packages has put greater demand on dielectric material to perform under diverse and extreme application conditions. Next generation of dielectric materials are required to demonstrate high resolution capabilities along with excellent electrical and mechanical properties. Reliability and integrity of a device under manufacturing as well as extreme service conditions depends on strong adhesion between organic dielectric film and all interfaces it shares with a diverse class of materials that are integral part of a device.

In this paper we will demonstrate correlation between adhesive strength of a photoimageable dielectric film and reliability. Reliability will be determined under biased- and un-biased HAST conditions as well as HTS performance after 1000 hours of storage at 150˚C. Photoimageable film (PID) of the study can be cured at temperatures below 180˚, with less than 5% film shrinkage under curing conditions, resulting in <15MPa residual stress. The PID film is based on fully cyclized polyimide platform that has demonstrated resolution capability down to 3 micron contact hole. Mechanical and electrical properties of the material are typical of a polyimide platform.

9:45 – 10:15 Coffee Break in Exhibit Hall

10:15 – 10:40 AM Colonial Room

"Volume Production Testing of Silicon Photonics Modules Case Study: Wafer Sort Test Coverage versus Through-Put", John Ritchie - Straits Hi-Rel Pte. Ltd. Singapore

Lowering Cost-Of-Test during volume production of Silicon Photonic products is directly proportional to lowering the Cost-Of-Manufacturing. A high-volume production test strategy which employs little or no wafer level test coverage prior to packaging results in low yield final assembly products. The cost of packaging defective die significantly increases the overall Cost-of-Manufacturing for the yielding final assembly products.

Employing a stringent full coverage wafer level test strategy during the production test process results in lengthy test times & very low through-put. This test strategy minimizes the possibility of packaging defective die, but due to the low through-put contributes to a significantly higher Cost-of-Test.

This case study describes a silicon photonic high-volume wafer sort test strategy which was implemented with the key objectives of: (1) providing enough wafer level test coverage to minimize packaging defective die; (2) maximize the wafer level test through-put; and (3) minimize the overall Cost-of-Test and Cost-of-Manufacturing.

10:40 – 11:05 AM Colonial Room

"An Electrical Fan-Out Wafer Level Packaging Test Vehicle and Update on the Advanced System Integration Program", John Allgair PhD , Amit Kumar, and Ankineedu Velaga – BRIDG, NeoCity, FL

The on-going advance of microelectronic based activity, including mobile devices, edge computing, connected sensors and cloud-based operations, is driving the semiconductor industry to come up with faster devices and smaller form factors. The traditional route to CMOS miniaturization via device level scaling is reaching its limit. The need for next generation smart sensors and other advanced devices is steering the semiconductor industry to look at the integration of materials beyond silicon. To address these challenges, the advanced system integration program at BRIDG is aimed at developing solutions through innovative technologies aimed at package level scaling and heterogeneous integration on a conventional silicon platform.

The Ultra High Density Interposer project is a multi-year activity focused on developing stacked interposers with signal input/output (I/O) an order of magnitude higher than typically achieved. In this phase, a multi-chip daisy chain circuit is defined that will allow testing via continuity, humidity, and thermal cycling to demonstrate the integrity of the interconnect layers, underfill and overmold. An overview of the design and initial process integration results will be presented. A status overview of the advanced integration program being pursued at BRIDG will also be provided.

Lunch 11:30 – 1:00 PM in Exhibit Hall

Session B: Printed Electronics

Chaired by Mary Herndon (Raytheon IDC) & Jim G. King (King Technologies)

Cotillion Room - 8:30 AM – 11:05 AM

8:30 – 8:55 AM Cotillion Room

"Curing Printed Conductive Layers on Low-Temperature Substrates with Intense Pulsed Light", Guinevere Strack, Andrew Luce, Craig Armiento, and Alkim Akyurtlu - Electrical and Computer Engineering Department, Printed Electronics Research Collaborative, UMass Lowell, Lowell, MA

Printed electronics is a branch of additive manufacturing that enables rapid prototyping and low-cost fabrication of devices for a wide range of applications, including antennas and other RF/microwave components. Although several materials and approaches are used in printed electronics manufacturing, the focus herein will be the application of intense pulsed light (IPL) to conductive inks printed on flexible substrates. IPL enables the rapid curing of printed conductive inks on the order of milliseconds over a large area and can be applied in roll-to-roll processing. This transient processing allows thin films to achieve high temperatures on a wide range of low-temperature substrates, such as thermoplastics, textiles, and paper. During this process, light is absorbed by the metallic ink, which causes a rapid temperature increase that removes insulating organic constituents or sinters the film into a single component. This process is affected by several factors, including the chemical and physical characteristics of the ink and substrate, the applied energy density, and the pulse parameters. Metallic ink composition can range from stabilized silver or copper nanoparticles to metal–organic complexes that decompose in the presence of heat and light. In addition to sintering, IPL can induce a chemical change in the ink, for example, the reduction of copper or silver. This presentation will focus on the application of IPL to silver and copper inks printed on flexible substrates and how the ink composition, substrate material, and IPL parameters effect the DC conductivity and RF performance of the conductive film.

8:55 – 9:20 AM Cotillion Room

"Testing Methodology and Analysis of Fusing Current of Printed Conductive Inks on Dielectric Substrates", Elicia K. Harper, Emily K. Engel, Susan C. Trulli, and Kara P. Upton - Raytheon Integrated Defense Systems, Andover, MA

Printed electronics and additive manufacturing (AM) are becoming more prevalent in microelectronic packaging for RF devices due to the low cost of fabrication, ease of customization and the advantages of rapid prototyping. One benefit of AM in microelectronic packaging is the ability to write DC & RF interconnects with conductive ink. Characterization of new materials for AM is an important part of the process to leverage this new technology, yet significant work has not been done in determining the DC handling capability of printed conductors. This work outlines a process for sample preparation and a methodology for determining the fusing current of various conductive inks. Inks were printed onto various dielectric substrates and sintered using different curing processes. Four-wire measurements were performed and different current levels were applied to the samples until the printed line fused. Based on the measured fusing current, the temperature rise of the line is extracted through equations and compared to thermal simulations. This presentation compares the fusing current of printed traces of different inks based on various substrates and curing methods.

9:20 –9:45 AM Cotillion Room

"Barium Strontium Titanate Nanocomposite Dielectric Inks for Flexible RF and Microwave Electronics Applications", Oshadha K Ranasingha, Mahdi Haghzadeh, Craig Armiento, and Alkim Akyurtlu - Electrical and Computer Engineering Department, Printed Electronics Research Collaborative,
Raytheon – UMass Lowell-Research Institute, Lowell, MA

The Applied Physics group at United Technologies Research Center (UTRC) is developing printed electronics methods, materials and acumen to spearhead proliferation of direct write, additive and automated high volume manufacturing methods throughout United Technologies Corporation's (UTC) business units and product offerings. UTRC and Pratt and Whitney are advancing direct write methods for in-situ measurement of critical engine parameters which previously could only be estimated. Work in novel functional materials formulation and supporting process development are enabling integrated sensing, validation and electromagnetic functionality in components across UTC Aerospace Systems in new ways which are only just beginning to be explored. High-volume, printed electronics techniques for flexible and in-mold applications are poised to transform the wearable electronics and automotive / white-good touch control industries.

The UTRC team is leveraging and evolving these techniques for implementation in buildings and aircraft environments empowering seamless manufacturing, packaging and human interactions with UTC's future products and systems. Advanced additive electronics manufacturing and packaging techniques will change the way we make and interface with our machines and UTRC is working as part of broad community to effect those changes. As a member of NextFlex (and other national manufacturing institutes), UTRC is teaming to develop autonomous printed electronics sensor platforms designed to help ensure the well-being of our people and perishable cargo.

9:45 – 10:15 Coffee Break in Exhibit Hall

10:15 – 10:40 AM Cotillion Room

"Printed Phase Shifters for Antenna Arrays", Shokat Ganjeheizadeh Rohani, Mahdi Haghzadeh, Craig Armiento, and Alkim Akyurtlu, Electrical and Computer Engineering Department, Printed Electronics Research Collaborative, Raytheon – UMass Lowell, Lowell, MA

This work presents design and fabrication processes for creating fully printed flexible phase shifters for conformal flexible hybrid phased array antennas. In our previous work, a fully printable and conformal antenna array on a flexible substrate with a new Left-Handed Transmission Line (LHTL) phase shifter based on a Barium Strontium Titanate (BST)/polymer composite ink was computationally studied for radiation pattern correction and beam steering applications. In this work, additive manufacturing techniques were used to demonstrate experimentally phase shifters for beam steering capabilities for a planar array. An Aerosol Jet direct-write printer was used to print phase shifter with the BST ink that were integrated with a series fed antenna array. This talk will describe the design of the series fed array, design of the phase shifters, and details of the fabrication process will be described. Specifically, details of the optimization for the phase shifters and the resulting experimental results will be shown. This work demonstrates the specific technologies including direct writing processes for flexible antenna arrays and integration of low cost printed phase shifters.

10:40 – 11:05 AM Cotillion Room

"Novel Techniques for Additive Manufacturing of Functional Materials", L. Parameswaran, , R. Mathews, L.M. Racz, Duncan, M. Plaut, T. Fedynyshyn - MIT Lincoln Laboratory, Lexington, MA; Y. Kornbluth, L.F. Velásquez-García, Massachusetts Institute of Technology, Cambridge, MA; B. S. Uzel, R. Weeks, and J.A. Lewis - Harvard, Cambridge, MA

Additive manufacturing technologies promise to transform the development and production of agile microsystems, but are limited by the ability to print functional materials. This talk will describe progress in the development of novel techniques and classes of materials enabling 3D printing of microelectronic
quality interconnect and low-loss dielectric composites.

State of the art 3D printing techniques for conductors cannot yet deliver the feature resolution and electrical conductivity required for high performance microcircuits, and have materials and substrate constraints, as well as post-processing requirements. We describe recent results in the development of a novel atmospheric microplasma sputtering system that can provide direct-write capability of metal interconnects on non-standard substrates, with future extensibility to dielectrics and semiconductors.

We have also developed new classes of 3D-printable low-loss dielectric polymers, ceramic composites, and conductors based on a triblock copolymer system that combines the properties of the matrix and filler components. These hybrid organic/inorganic materials exhibit good electromagnetic properties and we discuss the performance of RF devices that have been demonstrated to operate in the millimeter-wave range (>30 GHz).

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Lunch 11:30 – 1:00 PM in Exhibit Hall

Session C: RF & Microwave – Innovations & Microwave Emerging Technologies I

Chaired by Tom Terlizzi (GM Systems LLC) & Chandra Gupta (Comm. & Power Industries, LLC)
Seminar Room - 8:30 AM – 11:05 AM

8:30 – 8:55 AM Seminar Room

"100nm GaN on Si Technology for 5G Applications", Charles Edoua, OMMIC, Limeil-Brévannes Cedex France

5G has reignited a race amongst competing semiconductor technologies for inclusion in next- generation amplifiers, among which gallium nitride (GaN) is a major contender due its high power and temperature handling capabilities. In this workshop, we will address the prospects of GaN for new radio 5G (NR-5G) by tackling the full range of devices to systems opportunities and challenges. This begins with a comparison of the leading GaN MMIC technologies that are distinguished by the substrate of choice, namely GaN-on-Si and GaN-on-SiC. Trade-offs in material and device performance, as well as cost, will be addressed, as well as examples of current and upcoming MMIC designs for the market. Due to the high power of GaN MMIC modules and its relatively young age, reliability and packaging are critical. We will therefore present approaches to satisfy both the RF and thermal performance demands of GaN, alongside examples of hybrid GaN PAs.

8:55 – 9:20 AM Seminar Room

"A Reconfigurable S/X-Band 25W GaN Power Amplifier MMIC", Charles F. Campbell, Kevin W. Kobayashi and Cathy C. Lee - Qorvo Infrastructure and Defense Products, Richardson, TX

5G is the next proposed step in the evolution of wireless networks, providing an order of magnitude improvement in bandwidth delivered to the user device and enabling new vertical businesses for mobile operators. The ultra-broadband capability envisioned for 5G is based on both a move to higher frequencies (mmwave) and the evolution of MIMO in cellular bands.

Currently there are many field trials ongoing to test the 5G proposed architectures and validate the first wave of 5G specifications. As we move forward to implement there are many challenges to be overcome by the RF and microwave design community to make 5G a reality. Will breakthroughs in mmwave technology enable a whole new cellular infrastructure, or will we see a massive deployment of massive MIMO in sub 6GHz spectrum? In many ways, the future of 5G relies on us, the RF engineering community to deliver the advanced technology of tomorrow.

Let's take this journey into the future together. During this presentation we'll start by briefly discussing the 5G industry goals and motivations. Then we'll review the technologies that are in development today enabling the early 5G radio designs and we'll highlight some of the challenges that lay ahead for the RF design community including efficient radio circuits and architectures as well as integration and packaging.

9:20 – 9:45 AM Seminar Room

"GaN-on-Silicon for 5G Radios", Timothy Boles – MACOM Technology Solutions

5G promises to bring about another wave of performance enhancements that will not only significantly impact the way that we communicate, but will also call for major overhauls of the telecommunications infrastructure. This has reignited a race amongst competing semiconductor technologies for inclusion in next-generation amplifiers, among which gallium nitride (GaN) is a major contender due its high power and temperature handling capabilities. In this paper, we will address the prospects of GaN for new radio 5G (NR-5G) by tackling the full range of devices to systems opportunities and challenges.

This begins with a comparison of the leading GaN MMIC technologies that are distinguished by the substrate of choice, namely GaN-on-Si and GaN-on-SiC. Trade-offs in material and device performance, as well as cost, will be addressed, as well as examples of current and upcoming MMIC designs for the market. Due to the high power of GaN MMIC modules and its relatively young age, reliability and packaging are critical.

Approaches to satisfy both the RF and thermal performance demands of GaN, alongside examples of hybrid GaN Pas will be presented. In addition, a comparison to alternative/competing technologies needs to be considered relative to these GaN based efforts with the advantages of GaN technology for 5G clearly enumerated. The incumbent technology for 4G systems has been silicon LDMOS. It is hard to believe that the manufacturers that have made the

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large investment in this very successful technology platform will just walk away from the 5G opportunities, especially at frequencies below 6.0 GHz. As the 5G frequency bands move into mmW frequency realm, traditional GaAs based PA's and SiGe BiCMOS have the possibly of providing competitive solutions. This is especially true for GaAs which is already the PA technology of choice for point-to-point applications through 40 GHz. As 5G considers to massive MIMO/phased array solutions above 60 GHz and the required output power per element drops, SiGe BiCMOS will clearly offer completion to GaN based technologies.

9:45 – 10:15 Coffee Break in Exhibit Hall

10:15 – 10:40 AM Seminar Room

"Advancement in TPG Graphite Based Technology for Chip-level Thermal Management", Wei Fan, Liu Xiang, Brian Kozak, Kristi Scherler, and Greg Shaffer – Momentive Performance Materials, Inc., Strongsville, OH; Garry Wexler – Henkel Corporation, Prescott, WI

Thermal management is an increasingly challenging problem in today's microelectronics industry, especially during the transition to GaN and SiC devices. As power requirement increases and available space decreases, innovative materials with high thermal conductivity (TC) and light weight are desired to remove the critical heat. Thermal Pyrolytic Graphite (TPG), a unique synthetic material produced by Momentive via chemical vapor deposition, contains millions of layers with highly-oriented stacked graphene planes and exhibits excellent in-plane thermal conductivity (>1500 W/m-K) and very low density (2.25 g/cm3). TPG composite using metal encapsulation, such as TC1050 heat spreader, TMP-EX heat sink, and TMP-FX thermal straps, simultaneously achieves high thermal conductivity from the TPG core and mechanical integrity from the metal shell. TMP-EX heat sink, with options of both high in-plane and through-plane thermal conduction, was developed particularly for chip-level thermal management. We would like to share with the community our studies in RF and LED applications which revealed 50~60% more power loadings was achieved with TMP-EX heat sinks. In addition, an integrated TPG-core insulated metal substrate (IMS) solution is being explored in a joint effort between Momentive and Henkel. Prototypes of single layer and multilayer IMS structures using TMP-EX as substrate material were produced and their thermal performance was demonstrated. The integration of TPG and IMS paves a new route for adding thermal loading, improving reliability, simplifying module design and reducing assembling cost/steps.

10:40 – 11:05 AM Seminar Room

"Think Outside The Cylinder", Richard Howell - Cornell Dubilier / TTI, Inc., Boston, MA

A discussion of recent innovations and advancements in capacitor technology from Cornell Dubilier. Featuring new and in development flat packaged aluminum electrolytic options to replace wet tantalum capacitors while meeting critical high temperature, high vibration, weight and space saving metrics.

Session D: Interconnects

Chaired by Lee Levine (Process Solutions Consulting) & Bill Boyce (WBoyce Consulting)

Directors Room - 8:30 AM – 11:05 AM

8:30 – 8:55 AM Directors Room

"The Use of Designed Experiments in Process Development", Lee Levine - Process Solutions Consulting, Inc., New Tripoli, PA

Manufacturing semiconductor packaging requires a multitude of processes, many using high speed automatic equipment. Individual processes often have hundreds of programmable process parameters that can significantly affect yield, reliability and long-term quality. Wire bonding is one such process. Trillions of wires are bonded annually connecting semiconductor devices to the outside world. Wire bonding is a welding process. Currently as many as 25 wires/second can be bonded using state-of-the-art automatic machinery. The wires are bonded sequentially, each wire (2 welds and loop formation) is produced in 25mSec or less. Statistically designed experiments (DOEs, designed experiments) are the best method to understand, develop, and optimize the process. Designed experiments allow adjusting multiple variables simultaneously. During data analysis the effects of each variable are separated and tested to determine whether the differences between the levels of each variable have a statistically significant effect on the process response. In addition, many DOE designs are capable of measuring variable interactions. Often interaction

effects can be very important in understanding process behavior. Statistical validity testing improves data based decisions, avoiding false conclusions on small amounts of data.

This short course will discuss the use of Taguchi, Factorial, Fractional Factorial designed experiments as a method for understanding complex manufacturing processes. Examples from wire bonding will be used as the core but any process can as easily be studied. It will include selection of variables, choosing ranges and determining sample size.

8:55 – 9:20 AM Directors Room

"Zero Outgassing and Flux Residue Compatible Underfill", John Yin*, Mary Liu and Wusheng Yin, PhD - YINCAE Advanced Materials, LLC, Albany, NY

INFO (Integrated Fan out package) has been implemented in the semiconductor industry now. There are a lot of cleaning steps in wafer-level integration process. In order to avoid underfill contamination of neighboring components underfill has to have zero outgassing during underfill process even though this is very challenging requirement. It will be ideal underfill to be compatible with flux residue, in another word, the underfill can be used without cleaning flux residue.

The automotive industry is currently very hot due to the self-driver and flying cars. The reliability of the microchip such as BGA, CSP and other modules for automotive industry is much higher than the consumer industry. Therefore, the underfill is requested not only to enhance mechanic strength but also to absorb the stress from CTE mismatch. On the other hand, the flux residue has to be cleaned to achieve the best reliability of underfill. In addition, cleaning flux residue has becoming more and more difficult due to the density and miniaturization of components.

In order to address the issues occurred in the advancement of electronic industry, YINCAE has successfully developed zero outgassing and flux residue compatible underfill – SMT 158HA. This underfill has not only demonstrated high reliability but also can be used without cleaning flux residue and is fully compatible with flux residue. This underfill has demonstrated zero outgassing during underfilling curing step. After underfill curing, the electronic device can pass 5x 260°C reflow process. In this paper we discuss flux compatibility, outgassing and reliability in detail.

* Shaker high school student, intern at YINCAE.

9:20 – 9:45 AM Directors Room

"Introduction of Die Attach Hybrid Silver Adhesive Technology", Koyo Kobori – Tanaka, Kikinzoku Kogyo, Japan

New field of hybrid sintering die attach material updated constantly. Power semiconductor industries experiences radical improvement and package structure is getting complicated, smaller size and large capacity. As a solution it designed by thin die for heat dissipation. Therefore, conventional silver sintered material was developed low temperature and pressure less dispensing process by fine filler and so on. However, it is facing issue fillet height for thinner die using dispensing die attach process.Lead frame printing process is one of solution for creeping with thin die.
The purpose of this study suggest concept hybrid sintering material, characteristic, reliability and solution for fillet height with die attach process. In particular, in terms of dispensing and printing process with production equipment as printing machine and die bonder describe hybrid sintering material solve fillet height in house device. For characteristic assessment method is thermal conductivity by lase flash and hot die share strength by DSS machine various chip size with backside metallization on silver plated, PPF and cupper lead frame and failure mode. Assembled product observe reliability test up to 2000cycle by SAT. Furthermore, process evaluation is dispensing with die attach machine and printing as well. Tack time, staging time and voids check by hot die shear strength and X-ray.

9:45 – 10:15 Coffee Break in Exhibit Hall

10:15 – 10:40 AM Directors Room

"A Critical Review of MIL-STD-883 Wirebond Visual Inspection Criteria", Thomas Green - TJ Green Associates LLC, Bethlehem PA

Wirebond engineers and technicians primarily rely on three means by which to evaluate the integrity and reliability of a wirebond interconnect. Destruct/non-destruct pull test, ball shear, cross-sections, intermetallic coverage under the ball are tests used to evaluate the mechanical strength as part of process development and in line process controls. Reliability testing and evaluation involves these same tests after prolonged environmental exposure such as, temp

cycling, burn-in, humidity testing etc. according to standards such as AEC-Q100. Much has been written about the above. A third and very important consideration in wirebonding is visual inspection of the deformed wire after wirebond formation. The amount of wire squash-out, placement of the bond on the pad relative to nearby circuitry, looping profiles and heel integrity are all very important aspects of wirebond interconnect inspection. Poor workmanship can lead to noncompliant bonds per visual inspection criteria and can directly impact the reliability of the finished product. Bond pad inspection prior to bonding is also a critical aspect that is often overlooked. Historically, MIL-STD-883 has served as a baseline set of visual specs related to wirebond, and package assembly in general. Many company quality documents reference MIL-STD-883 TM 2017 and TM 2010 and/or cut and paste the bond inspection criteria into internal documents. This paper critically reviews the wirebond visual inspection criteria contained in MIL-STD-883 relative to the requirements of a fully optimized modern day wirebond process.

Key Words: MIL-STD-883, Visual Inspection, TM 2017, TM 2010, Workmanship Standards eBook Hybrids Microcircuits RF/MMIC Modules workmanship standards

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10:40 – 11:05 AM Directors Room

"Introduction of Copper Alloy Bonding Wire for the High Rel Industry", William Crockett Jr. – Tanaka, Japan

Since around 2008, the shift from Gold (Au) bonding wire to Copper (Cu) bonding wire has been taking place on full scale with the aim of reducing costs. When compared with Au, Cu wire presents challenges in reliability and repeatable bonding characteristics in terms of chemical stability, which is required in high reliability applications. Therefore Cu wire adoption in automotive and industrial semiconductors has been limited. Conventionally, the market of Cu bonding wires has been divided into two types: bare Cu wires (high purity) and palladium coated (PCC) bonding wires. These wires have yet to satisfy the required characteristics for high reliability products such as industrial and automotive electronics.

A new bare Cu alloy wire offers competitive advantages for high reliability applications with reliability improvements of 1.5 times conventional bare copper wire. As a result of testing the failure rate at the high temperature of 175 degrees Celsius, it was found that the failure rate of conventional bare copper wire started rising after 800 hours, Cu alloy wire maintained a failure rate of 0% even after 1,200 hours, confirming that it has 1.5 times the reliability of conventional bare Cu wire. With the reliability 1.5 times than conventional bare Cu products, Cu alloy wire excels in all aspects of productivity, bondability, cost and electrical conductivity. In addition, Cu alloy wire can achieve higher productivity on 2nd bond process and no damage to aluminum electrodes on IC chips due to the optimization of ball softness

Cu alloy wire is able to significantly reduce manufacturing costs while sufficiently meeting the required performance by replacing the currently widely used gold wire in applications requiring high reliability, such as automotive electronics, industrial electronics and military high reliability applications. Costs can be further reduced by 20% when compared to PCC wires.

Will Cu alloy wire gain acceptance in the high reliability electronics? Stay tuned…

Lunch 11:30 – 1:00 PM in Exhibit Hall

Keynote Lunch Address

"General Applications of AESA Radar Technology"

Presented by Gerald (Jerry) Charlwood

Director, Lightwave Antenna Business Unit – MACOM

11:50 AM – Exhibit Hall

Afternoon Technical Program

Session F: Novel Packaging Applications
Chaired by Jim Ohneck (Laser Therapy Services) & Rick Elbert (Cicor Group)
Colonial Room - 1:00 PM – 3:05 PM

1:00 – 1:25 PM Colonial Room

"Medical Imaging Applications - the Underlining Technology", Dan Negrea – AEMtec GmbH, Berlin, Germany

Presently four key detection technologies are dominating the medical imaging market: the CT detection, the PET detection , the MRI and the Ultrasound. The fundamental differences between these technologies consists in the very nature of the transducers or sensors used in each type of application.

Besides this first functional layer – the transducers – the manufacturing technologies used to assemble these transducers in modules, directly useable in the different devices, are facing largely identical challenges, the main ones being the accuracy of the assembly, the planarity of the surface in case multiple tiles are being used, the low-stress assembly and of course the long-term reliability. In case multiple tiles are used and the final image is calculated through interpolation, it is a huge advantage to have as few as possible rows of missing pixel to interpolate. This can be achieved through accurate tiling, for instance with an accuracy of ¼ pixel.

The planarity of the surface when tiling in involved, solves at least two key problems: most photonic sensors used in CT (in case they do not perform direct conversion), require a glued scintillator ceramic on top of the sensor. An uniformly thick layer of glue offers better sensitivity calibration and better interchangeability possibilities. The ideal sensor has a high sensitivity for the signal to be measured and is immune to other environmental factors. Real life is different: environmental factors like internal tensions in the chip may largely affect the performance of the used sensor. A stress-free assembly brings huge advantages in terms of thermal drift, gradient of sensing performance over the surface and long-term stability.

In Berlin we produced in the past 10 years hundreds of thousands of different types of highest-end sensors with very high yield and long-term reliability.

1:25 – 1:50 PM Colonial Room

"Fully Organic Packaging for Applications with Liquid Exposure", Susan Bagen - Micro Systems Technologies, Inc., Lake Oswego, NY; Eckardt Bihler, Marc Hauer - MST Dyconex AG, Bassersdorf, Switzerland

Liquid Crystal Polymer (LCP), a thermoplastic dielectric material with very low water absorption (< 0.04%), high chemical stability and low thermal expansion is best suited both as a substrate material and as the encapsulate for small miniaturized electronic packages and modules. LCP stands out among other polymer materials used for microelectronics. The permeability for water and gases is the lowest among all polymeric materials. With proper design considerations LCP packages can achieve a sufficient low permittivity for exposures in liquid media.

Processing techniques for LCP substrates are the same as for other packaging substrate materials. Resolution of lines, spacing and vias are comparable. Multi-layer structure with thin dielectric layers can be made using LCP films.

1:50 – 2:15 PM Colonial Room

"Advancement in Microelectronic Packaging for Medical Implants", Caroline K. Bjune - Draper Laboratory, Cambridge, MA

In the world of electronics, the call for more and more functionality comes with the expectation of maintaining the current footprint or even better, reducing it. Advancements in microelectronics design and packaging have been one of the major factors in meeting these demands. Device and system packaging for medical implant applications is no different. Many believe that miniaturization is key to developing implantable products that have minimal adverse impact on quality of life. In this talk, approaches in microelectronics packaging taken for several systems will be discussed. Applications including a cranial mounted neural interface, peripheral nerve interface for advanced

prosthetics, and ultra-miniaturized neural stimulator, will be discussed. Packaging, assembly, and materials trade-offs will also be discussed.

2:15 – 2:40 PM Colonial Room

"Think Like an Innovator, Act Like an Entrepreneur", Angelique Johnson, MEMStim LLC, Louisville, KY

We often wonder why so many microelectronic innovations never make it beyond science fiction, and yet a plethora of seemingly useless products are brought to market every day (i.e. fidget fingers). Academic innovators are frequently hyper focused on scientific discovery and entrepreneurs on profit. However, commercialization resides at the intersection of profit and discovery. An overindulgence of either creates a valley of death between them. In this talk, Dr. Angelique Johnson will share her experiences overcoming commercial challenges with medical MEMS innovation, while at the same time letting her commercial actions be driven by the market demand. Johnson will cover best practices on pulling the two mindsets together and avoiding chasm-building mentalities that lead to the valley of death for many medical microelectronic implants.

Biography: Dr. Angelique Johnson is CEO/founder of MEMStim LLC, and has raised nearly $2.5 million in non-dilutive funds to commercialize microfabricated nerve stimulators. An expert in Lean Startup Methodology, she has educated students on building successful companies. With a doctorate in Electrical Engineering from the University of Michigan, she is an authority on innovation and entrepreneurship. Dr. Johnson has delivered a congressional briefing on Capitol Hill, served as a speaker for the eighth district of the Federal Reserve, and delivered several international talks. She has been featured on NBC Universal, National Public Radio, The Root news site, Louisville Insider, Business First, and other media outlets.

2:40 – 3:05 PM Colonial Room

"Fabrication and Packaging of a MEMS Based Energy Harvester", Yuechen Yang, Ujwal Radhakrishna, Dennis Ward, Anantha P. Chandrakasan, Jeffrey H. Lang - MIT, Cambridge, MA

A prototype electromechanical MEMS based-transducer is fabricated using a combination of lithography, 3D printing, and machine shop techniques. The transducer spring bed design uses a modified version of the classic 4 bar linkage spring design, the long beams are tapered to reduce stress, such that the end connecting to the guide rod is wider than the connecting region to the shuttle, which houses the magnet. The transducer spring bed is made from silicon with a deep reactive-ion etching process. This process allows for near vertical sidewalls, which increases device efficiency. The transducer is housed in a series of 3D printed plastic package parts. The top and bottom parts houses the coils, which are fixed in place using paraffin wax. The middle insert houses the spring bed containing the magnet. The parts come together to provide the desired spacing between the magnet and the coils. The coils are manually wound using 44 AWG enamel coated copper wires on a custom made mandrel. With two coils placed at the desired distance above and below the magnet's plane of motion. When attached to the source of vibration, the magnet vibrates in between the coils, inducing an EMF in the coils in accordance with Lenz's Law. The coils are connected in series and the induced voltage adds to produce an output voltage, which is interfaced with custom designed circuitry for energy harvesting. The assembled mechanical harvester is capable of delivering 1mW of output power at resonance with a matched load.

Session G: Photonics & Optoelectronics Packaging
Chaired by Yi Qian (MRSI Systems) & Jin Li (Cambridge Technology)
Cotillion Room - 1:00 PM – 3:05 PM

1:00 – 1:25 PM Cotillion Room

"The Evolving Face of Integrated Photonics: New Packaging Strategies", Juejun Hu, Shaoliang Yu, Haijie Zuo, Jerome Michon, Derek Kita, Sarah Geiger, Qingyang Du, and Tian Gu – MIT, Cambridge, MA

Often hailed as the counterpart of electronic integrated circuits in the optics domain, integrated photonics have emerged as a mainstream technology for applications covering communications, computing, sensing, and quantum information. Nevertheless, the demand for precise alignment, sensitivity to optical losses, and strong wavelength dependence pose significant challenges to packaging of integrated photonic circuits. In this talk, we will discuss

several examples of photonic packaging technologies and their applications. In addition, we will also introduce a new ultra-broadband, low-loss, and misalignment-tolerant optical packaging design based on 3-D free-form micro-optics.

1:25 – 1:50 PM Cotillion Room

"Quantum Dots in Long Wavelength Applications", Xifeng Qian, Elif Demirbus - UMass Lowell, Lowell, MA

Since the realization of quantum dots (QDs), it has shown great potential in optoelectronic applications due to its unique properties of 3-D carrier confinements. The rapid progress of QD devices has brought to the demonstration of quantum dot lasers, quantum dot infrared photodetectors (QDIPs), amplifiers and solar cells. This talk will discuss QD applications in long wavelength sources and detectors, such as QDIPs and QD cascade lasers, which are based on carrier intersubband transition mechanism in QDs. Moreover, we will introduce a novel design of mid-infrared lasers using strain-balancing QD and QW hybrid structure.

1:50 – 2:15 PM Cotillion Room

"Full-field Digital Holographic Vibrometry for Characterization of Optoelectronic Packaging and MEMS", Cosme Furlong, Payam Razavi, Morteza Khaleghi, and Ivo Dobrev - Center for Holographic Studies and Laser micro-mechaTronics (CHSLT), Mechanical Engineering Department, Worcester Polytechnic Institute, Worcester, MA

Development of quantitative full-field high-speed imaging modalities are indispensable to monitor the realtime transient performance of Micro Electro Mechanical Systems (MEMS). Their performance is a direct result of how devices are designed and fabricated and any imperfection in either one of them renders undesirable results. Furthermore, new devices are being designed to comply with tighter performance tolerances while operating at higher speeds. In this paper, we report progress in the development of a new High-speed Digital Holographic System (HDHS) for acquisition and quantification of the nanometer scale transient (i.e., >100 kHz) displacement of MEMS in full-field. We have optimized and implemented a 2+1 frame local correlation (LC) based phase sampling method in combination with a high-speed (i.e., >100 kfps) camera acquisition system. Comparisons of the results obtained with our high-speed acquisition system and those obtained with Laser Doppler Vibrometry (LDV) indicate differences of <10 μs. The high temporal and spatial (i.e., >150 k data points) resolution of our HDHS enables parallel measurements of all points on the surface of microstructures, which allows quantification of spatially dependent motion parameters such as modal frequencies, time constants, Q-factors, changes in shapes, and surface strains. Such capabilities allow inferring performance parameters that can directly be used to improve MEMS design and fabrication as well as to optimize their corresponding mechatronics and control systems. Representative applications of our HDHS to study specific high performance MEMS will be presented.

Keywords: high-speed digital holography, MEMS design and fabrication, MEMS performance, transient events.

2:15 – 2:40 PM Cotillion Room

"Industrial Automation Sensors and Industrial Internet of Things (IIOT)", Yongyao Cai - Rockwell Automation, Chelmsford, MA

Recently Industrial Internet of Things (IIOT) has been a very hot topic and attracted heavy investment from every major industrial players. Different from a boarder concept of Internet of Thing (IOT), it focuses on interconnection in industrial space. It brings machine, people and analytics together at work. Industrial sensors, often thought as the eyes of industrial automation, is a crucial part of IIOT. Industrial sensors includes photoelectric sensor, inductive proximity sensor, capacitive sensor, magnetic sensor, and many others. Such technology allows physical information of machine and people be collected and transferred to a control unit, and eventually feed into analytics and preventative maintenance. As IIOT develops, solution providers are looking for more information than traditional industrial sensors can provide. New generation of smart sensors with digital communication capability is providing a lot more value than before. Such new development places new requirements and challenges to industrial sensors.

2:40 – 3:05 PM Cotillion Room

"High-Speed, High-Precision and High-Flexibility, Automated Die-Bonder for High-Power Laser Diode (HPLD) Packaging", Rajiv Pandey, Jason Liu, Julius Ortega, – MRSI Systems, N. Billerica, MA
High-Power laser diodes (HPLD) are one of the fastest growing segments in the laser industry driven primarily by growth in fiber lasers where HPLDs are used as pump sources. However, as fiber laser market prices continue to

decline and approach commoditization, HPLDs are forced to follow the same trajectory. To satisfy this growing demand while maintaining their profit margins as prices continue to decline, HPLD manufacturers are under pressure to reduce manufacturing costs through automation. Furthermore, HPDL packaging form factors lack standardization making automation challenging. To address these manufacturing challenges, MRSI has designed and developed the H3-series of automated die-bonder that can deliver the flexibility and precision without sacrificing throughput for maximum asset utilization. MRSI's HPLD eutectic die-bonding process delivers a highly reliable bond with low% voiding, high bond strength, low stress solder joint and high placement accuracy. This combination of equipment's capability and process optimization ensures that the end-user can mount the HPDL on its carrier with the highest reliability. This presentation describes the key features, benefits and value proposition delivered by this machine.

Session H: RF and Microwave – 5G Innovations & Microwave Emerging Technologies II

Chaired by Stephen Bart (InvenSense SSBC) & Rick Morrison (Draper)

Seminar Room - 1:00 PM – 2:40 PM

1:00 – 1:25 PM Seminar Room

"Epoxy Preform Guidelines for RF Microwave Module Assembly", Scott MacKenzie, President - Bonding Source, Manchester NH

Conductive and insulating epoxy film options available to RF Microwave module manufacturers have increase dramatically over the last 15 years. Converting options are no longer limited to hand cutting small batches or die cutting high volume requirements. The advent of laser cutting preforms is now well established and offers a solution to the industry for any batch size. As module manufacturers become more sophisticated, preform converting has evolved to help improve module performance, process control, manufacturability, and overall quality. Effective pre-form drawings now contain information that is essential for meeting the requirements of demanding manufacturers. This presentation outlines these parameters and shares guidelines used by tier one defense and aerospace companies. The information is geared toward engineering, manufacturing, and quality professionals involved in RF microwave module design and assembly.

1:25 – 1:50 PM Seminar Room

"Thermoplastic Polyimide (TPI) Adhesive Technology for RF Circuit", Jim Fraivillig, Fraivillig Technologies, Boston, MA

Thermoplastic polyimide (TPI) adhesive provides robust bonding between substrates with a bondline thickness of only 2-8um (0.08-0.3 mil), even when the substrates have a severe CTE-mismatch (say, silicon on aluminum) and are repeatedly thermal shocked. TPI is compatible with surfaces of semiconductor, ceramic, metals (except unpassivated copper) and plastics. Like other polymeric bond lines, the TPI polymer can be filled with a high loading of inorganic material, such as silver flake (electrically conductive) or BN powder (thermally conductive, while electrically insulating, 140V/um). In its B-staged form, TPI thermo-compression bonding of semiconductor die to heat sinks or spreaders can be done in seconds.

1:50 – 2:15 PM Seminar Room

"Elevated Temperature Impact on Performance of LTCC Dielectrics", Anton Polotai, Jim Henry, David Thoss, Yi Yang, and Sanjay Chitale - Ferro Corporation, Independence, OH

An adoption of higher frequency telecommunication protocols, a growing need to incorporate control and monitoring systems next to heat generating units, plus a high demand for power electronics set new requirements for the temperature ranges at which electronic components need to operate. The majority of current materials for the electronic components was designed for a "traditional" temperature range, from -55°C to +125°C, whereas the new applications require electronics to operate reliably up to 350°C and higher. In the past, the need for specific design rules related to elevated temperatures for microelectronic applications were limited mostly to applications like aerospace and oil exploration. The total number of components needed for those applications was relatively low, which enabled engineers to individually design each component using a trial and error approach. Such an approach is costly and time consuming, but the risk of failure of the entire unit in those unique applications warranted additional

design costs. Nowadays, with limited time-to-market and a growing pressure to minimize manufacturing costs, a proper selection of the appropriate materials become even more important.

Low Temperature Co-fired Ceramic (LTCC) modules are multi-layer ceramic substrates, which are co-fired with low resistance metal conductors, such as Au, Ag or Cu, at low firing temperatures, less than 1000°C. LTCC materials are often referred to as "Glass Ceramics", because their main composition consists primarily of glass and metal oxide filler(s). LTCC materials are used for an integration of various electronic components to a single module or package. Signal propagation and electrical resistivity of the LTCC material are two of the most important aspects for the electronic packaging. The signal propagation delay, t_d, is a direct function of the relative permittivity of the ceramic, which surrounds the conductor lines, and can be expressed as

$$t_d \sim l\sqrt{\varepsilon_r}/c$$

where l is the line length, ε_r is the relative permittivity of the substrate and c is the speed of light. Thus LTCC materials with low relative permittivity are required to increase the speed of the signal. The electrical resistivity of the LTCC material governs not only frequency at which the package can reliably operate via the value of the dielectric loss, but also the package density via the size of the separation gap between the adjacent conductor lines. As the operating temperature elevates, the conductivity losses occurring in the glassy phase of the glass-ceramic LTCC material may not only significantly increase dielectric losses of the LTCC packages, but also contribute to the increase of relative permittivity of the ceramic, suppressing the signal propagation. Understanding the temperature impact on the electrical and physical properties of the LTCC materials is a good way to understand when the current design rules need to be questioned for higher temperature applications.

The goal of this paper is to evaluate how commercially available LTCC ceramic dielectric materials behave at elevated temperatures to gage their applicability for the high temperature application. The properties of two popular LTCC ceramic systems having different microstructure forming mechanisms, Ferro A6M-E and Ferro L8, were measured in the temperature range from room temperature up to 450°C. One dielectric (A6M-E) consists of a crystallizing glass while the other (L8) consists of a ceramic-filled glass composite. The two materials exhibited considerably different relative permittivity, dielectric losses, and insulation resistance dependence on the operating temperature suggesting different temperature applicability range for each of the dielectric.

2:15 – 2:40 PM Seminar Room

"Reliable Sealing of Metal Packages", Tom Salzer – Hermetric, Inc., Bedford, MA

This article addresses hermetic weld sealing of semiconductor devices, considered by many to be an important legacy technology from decades gone bye, and not currently relevant in today's arsenal of seal technologies. However, we will show that it is still used to seal various high power devices as well a high reliability semiconductors, crystals, photonic devices and hybrid circuit packages. Its popularity primarily stems from the fact that it can be used to quickly and efficiently produce true hermetic seals in components. The welding is so rapid, that it is essentially a room temperature technology and the equipment is small enough that it can be housed in a controlled chamber filled with any gas that is not explosive. Air, Nitrogen, Argon, Helium and their mixtures are the most common gasses. In some applications the technology competes against laser welding, but unlike laser welding the entire seal takes place in a few milliseconds because it is a single discharge component-shaped spot weld, which means that the entire seam is made in a single high speed discharge. This process results in minimal stress and distortion, and maximum hermetic properties, strength and reliability, without requiring electroplating or preforms. Internal dew points can be held to -40 degrees, or lower if required. Other common applications for this technology include sealing and welding of nuts and studs for hermetic applications and sealing of devices for medical applications that must endure autoclave sterilization. In the course this presentation, we will take you back to the roots of the origins of the original resistance welding process as taught by the original process developers so that you will see for yourself how things have changed, and the reasons for the changes.

Session E: Interactive Dialog Posters

Chaired by Dipak Sengupta (Analog Devices Retired), Michael Johnson (MACOM), & Dave Saums (DS&A LLC)

In Exhibit Hall – All Day Interactive Discussion Period: 2:00 – 4:00 PM

"Challenges in Solder Attaching an Air Cavity Device Using Tin Bismuth Solder", Michael Johnson - MACOM Technology Solutions, Lowell, MA

The most common solders to attach components are either Sn63Pb37 or a lead free solder such as Sn96Ag3Cu5. There are some cases that come up where a lower temp solder is needed whether it is due to the order of assembly process steps or temperature sensitivity to components inside a device. This particular application which will be shown involved the attachment of a laminate air cavity device required the use of a solder that had a max temp of 170 C due to the construction of a piece part inside the device and overall temperature sensitivity and reduction of movement due to CTE differences causing electrical performance issues. For this development two devices were selected, one with an embedded heat sink and one without a heat sink. In this particular case, tin bismuth solder was selected for its low melting temperature. Tin Bismuth solder has some known mechanical issues that include a low drop shock resistance, solder tends to be brittle, the solder tends to expand as it cools which can cause component lifting and a lower surface tension compared to standard solders which can affect the registration of the device. It will be shown how careful selection of the land pads utilized in the final design, stencil modifications due to flatness issues, dye penetrant testing to validate X-ray images, EDX analysis to confirm proper intermetallic can lead to a robust connection that allowed for the devices to pass qualification.

"Advanced Thermal and Embedded Solutions for Laminate Substrate Designs", Abimael Reyes, Eric Eilenberg, and Paul Hogan - MACOM Technology Solutions, Lowell, MA

As demand for high-powered solutions and smaller package footprints continues to grow, it drives the need for continued advancement of laminate based substrate technologies. Besides shrinking the conventional SMT component and utilizing high thermally conductive epoxies, advancing the laminate substrate is the next step to increase functional integration and reduce package footprint. By embedding active and passive components as well as utilizing alternative fabrication methods we can balance increasing functional density while mitigating thermal challenges. This poster will review and compare various thermal solutions including standard vias, slot vias, and embedded heat slugs from both a fabrication and thermal modeling point of view.

"Evaluation of the Thermal Performance of a Light Emitting Diode (LED) Package Manufactured Using POL-kW Packaging Technology", Anisha Walwaikar[1], Christopher Kapusta[2], Liang Yin[2], Kaustubh Nagarkar[3], Krishnaswami Srihari[1], Daryl Santos[1] - [1]Department of Systems Science and Industrial Engineering, SUNY Binghamton, NY; [2]GE Global Research Center, Niskayuna, NY; [3]GE Ventures, Niskayuna, NY

The thermal performance of an LED package is evaluated in this work. The research is conducted by using a modeling approach, followed by experimental analysis. Initially, thermal modeling/simulation software will be used to study the thermal performance of prototype designs with different substrates and geometry designs. The initial modeling/simulation effort will be utilized to select the substrate material and geometry parameters before an extensive prototyping process. Subsequently, the optimized prototype design will be validated by experimentally measuring the surface LED temperature using infrared (IR) microscopy.

"Transient Liquid Phase Bonding Technology of Bi-Ni System for High-Temperature Electronics", Hamid Fallahdoost and Junghyun Cho - Materials Science & Engineering Program, SUNY Binghamton Binghamton, NY

A novel transient liquid phase bonding (TLPB) was developed in Bi-Ni system as a reliable lead-free solder alternative. Homogenous bond was produced via isothermal solidification at reflow temperature that has higher working temperature. The bonding layer was prepared through i) sputtering deposition and ii) powder metallurgy technique. Mechanical properties were investigated by testing bonded samples under shear stress. Scanning electron microscopy and energy dispersive X-ray spectrometer were employed to characterize the detailed microstructure within the bonding area. It was shown that two intermetallic phases, Bi_3Ni and BiNi, along with the remaining Bi, are responsible for the properties of TLPB.

"Evaluation of Mechanical Properties and Adhesion of Various Conformal Coatings Used in Electronic Packaging", Preeth Sivakumar and Junghyun Cho - Department of Mechanical Engineering, SUNY Binghamton, Binghamton, NY

Conformal coatings can be used to mitigate tin whisker growth on tin-rich surfaces, for which its mechanical properties and adhesion will play a crucial role. In this study, various types of conformal coatings (acrylic, silicone, polyurethane, and polyurethane acrylate) were investigated under various curing conditions to measure mechanical properties and coating adhesion to tin surface. FT-IR, Raman spectroscopy and DSC were used to examine the degree of curing of the coating. Mechanical properties were evaluated by universal testing machine and micro-hardness testing. Furthermore, adhesion of the coating was determined by a cross-cut tape peeling test.

"The Effect of Solder Paste Volume on Surface Mount Assembly Self-Alignment", Pan[1], J. H. Ha[1], H.Y. Wang[1], I. Parviziomran[2], D.H. Won[2], S.B. Park[1] -[1] Mechanical Engineering,SUNY Binghamton, NY; Systems Science and Industrial Engineering, SUNY Binghamton, NY; [2]Koh Young Technology Inc., Seoul, Korean.

In the surface mount assembly, the inconsistency in solder paste volume and the placement of the component play a vital role in the movement of the chip components when they go through the reflow soldering process. These movements may lead to common assembly defects such as overhanging, tilting, nonwetting, and tombstoning. Components to be assembled in surface mount assembly have self-alignment nature. It is driven by the total internal energy including gravitational energy, surface tension energy, etc. in the molten solder attributed to various factors. The factors include 1) solder paste composition, surface energy, gravity; 2) process variations such as solder paste volume, solder paste location, the difference of solder paste volume on the two ends of the component, and components placement location and orientation; 3) design parameters such as pad dimensions, pad-to- pad spacing, and surface finish.

In this research, energy-based three-dimensional models were created to predict solder joint final shapes. Three types of passive chip components are chosen for the modelling examples to investigate the component self-alignment performance during the reflow soldering process. By nature, the molten solder being a bulk fluid always tends to minimize its internal energy towards mechanical equilibrium and causes the component to move to the state of minimal energy. This movement leads the component to self-align. Thus, by creating energy minimization models, we can simulate the process of component self-alignment and predict the solder joint final shape (profile), terminal location and orientation of the component.

An extensive number of experimental studies were performed to develop a data-driven prediction model. The passive components were placed with intended misplacements and their positions was measured before and after soldering. A wide range of surface mount assembly imperfections were considered and intentionally designed for our study to achieve a powerful dataset and better convergence. The predicted component movement from the experimental study was then compared with the simulated component movement for validation.

"A Study Of Substrate Models And Its Effect On Package Warpage Prediction", Van-Lai Pham, Huayan Wang, Jiefeng Xu, Charandeep Singh, Jing Wang, & Seungbae Park - Department of Mechanical Engineering, SUNY Binghamton, Binghamton, NY

In this work, a study of different substrate models on package warpage is performed. Three different substrate models are built: First, the package substrate is simplified and modeled as one effective layer. Second, a three-layer model is proposed with a top build-up layer, the middle that contains a low Coefficient of Thermal Expansion (CTE) core, and a bottom build-up layer. Third, a multi-layer laminate substrate that accounts for the complexity of copper trace, and the combination of polymer or non-metallic materials is considered. Package warpage among these models are compared and evaluated by both an analytical approach and Finite Element Analysis (FEA) in conjunction with the empirical data. The analytical and FEA results reveal that the three-layer model and multi-layer model could predict package warpage behavior in close approximation to the experimental results, whereas the one effective model provides an outlier quantity. A small amount of uncorrected warpage prediction may result in a large discrepancy of service life assessment of interconnected solder joints. The multi-layer model with detailed copper trace configuration is prohibitively expensive, while one effective layer could not represent correctly the major mechanical properties of the substrate; above all, the three-layer model is an optimal consideration and is recommended to have a proper FEA model for a more exact life prediction of solder interconnections.

"Time 0 Void Evolution And Effect On Electromigration", Jiefeng Xu[1], Scott McCann[2], Huayan Wang[1], VanLai Pham[1], Stephen R. Cain[1], Gamal Refai-Ahmed[2], S.B. Park[1 - 1] Department of Mechanical Engineering
SUNY Binghamton, Binghamton, NY; [2] Xilinx, Inc., San Jose CA

Nowadays, As the revolution of advanced packaging technic, such as 2.5D and 3D packaging. The electronic package has a shorter electrical path between different ICs and achieves more I/Os, in the meanwhile, the scale down of the package size led to a shrinkage of interconnect size and a significant increase in electrical current. This trend will result in higher current density and joule heating in the interconnections, which significantly enhance the Electromigration (EM) damage. In this regard, EM become a critical issue in the reliability of electronic packaging.

Solder and copper are two most common used conductor materials in a electronic package. Due to the material properties, solder is weaker than copper in EM perspective. In previous research, most of EM acceleration test for solder were performed at 150C and 104A/cm2 or higher, but, for copper, it was conducted at 350C and 107A/cm2 at least. In the meanwhile, time 0 void are easier induced and hard to avoid in solder joint during manufacturing process. This initial void have great impact on the EM, because EM failure will have the initial void and accelerated the void nucleation and grow process. There are rarely research shows relationship between time 0 void and EM.

In this report, both experiments and numerical were studied to investigate the time 0 void effect on EM in lead-free solder (SAC305) joint. We used X-ray to observed the time 0 void in the solder joint and then cross sectioned at the center of the void. Three void location on the substrate side were chosen, the first on is at the right corner near the current entrance site; the second one is at the left corner far away from the current entrance site, the last one is near the middle. The samples were placed in the oven chamber at ambient temperature 125C and stress at 12A. temperature and voltage was monitored in-situ to observe the change during the test. The tested sample pulled out and investigated the void and micro structure evolution per 50hrs. we found that void located at the corner near the current entrance site will significantly enhance the EM, Void will depleted the growth along the Cu-SAC interface; on the opposite, initial void will not change when a new void was formed on the current entrance corner, after that two voids would grow and merge together along the Cu-SAC interface; when the void near the middle, void would grow on both direction (left and right) along the Cu-SAC interface. Copper trace was depleted in all test cases. A Finite Element Analysis was performed based on the experiment. It shows that void at the corner will increase the current density and joule heating about 2 times than without void at the same time 0 void size. When the diameter of void larger than 20% of the open windows, the meat time to failure will significantly reduce not matter where the void located. Copper will be accumulated around the void to form CuSn. Overall, the simulation is well agreed with the experiment.

“Characterization of Silicon Die Filleting Process through Dispensing”, Ludovico Cestarollo, Mohammed Alhendi, Darshana Weerawarne & Mark Poliks – SUNY Binghamton, Binghamton, NY

Flexible hybrid electronics integrates rigid electronic components with printed features on flexible substrates, allowing the final product to stretch and bend while still preserving the operational integrity of conventional electronics. Components of various thicknesses may be placed on the substrate and, in order to be integrated with each other, robust electrical interconnections are to be printed between different leveled surfaces of the substrate. Rigid components present sharp edges that constitute points of high mechanical stress for the interconnects, which consequently are more likely to fail in these locations, rather than on the other flat surfaces on the substrate or on the top of the components. It is of crucial importance to effectively fillet the sides of the components, in order to create smoother surfaces that climb over the edges, offering a more robust solution for the printing of electrical interconnections.

Despite this concern is of crucial importance for several applications in flexible hybrid electronics, it has not received much attention in the literature. Gu et al. have published a paper in 2017 where they explain the process they have developed to fabricate aerosol jet printed fillets. However, in such a process where precision at the micron scale is not a concern, dispensing offers a more convenient solution than aerosol jet printing. In fact, dispensing can deposit large quantities of material at a much faster speed, still obtaining precise and repeatable results for the requirements of this kind of application. This paper presents the work done to characterize the dispensing process of die fillets using DuPont 5036 Encapsulant as the filleting material. Silicon dies were filleted using different levels of dispensing parameters of interest. Then, conductive lines were printed over the dies and the fillets using aerosol jet printing (AJP) technology, in order to assess the quality of the fillets. The quality was assessed through the resistance measurements of the AJP-printed lines; the larger the resistance, the worse the fillet. The experiment was conducted following design of experiment (DOE) rules, in order to determine which dispensing factors significantly affected the quality of the fillet. The optimal factor levels were defined, and the results of the DOE analysis were supported by laser microscopy analysis of the samples.

“Process and Reliability Investigation of Sn-Bi Assembly for BGA Components”, Chongyang Cai, Jiefeng Xu, Huayan Wang, Seungbae Park - Department of Mechanical Engineering, SUNY Binghamton, Binghamton, NY

Lead-free solder alloys are widely used in microelectronic fields nowadays due to the environmental problems and toxicity of SnPb solder alloys. With the miniaturization of electronic packages, the industry is putting higher demands on the reliability of solder joints. The eutectic SnBi solder alloy, with low melting temperature, is a possible alternate for Pb-free solder alloy. Low temperature soldering can not only save the energy for heating, but also can increase the reliability of joints by minimizing warpage during processing. Besides, it brings benefits for packages involving organic materials and can be used for heat sensitive devices. In this study, board level reliability of assembly for BGA components were investigated. Three types of assembly are compared: pure SnBi assembly, SnBi/SAC305 hybrid assembly and pure SAC305 assembly. 42Sn-58Bi and SAC305 balls are placed on BGA components with different size of pitch and ball diameter. All components are daisy chained to form circuit paths when assembled to PCB boards so that the resistance can be inspected. To study the reliability of solder connections, the thermal cycling test results of each kind of assembly are compared. The fatigue life and behavior of low melt joints comparing conventional SAC305 solder joints are discussed. This study provides guidance for low melt solder ball assembly processing and shows the influence of solder alloy on reliability of BGA joints.

"Product Level Design Optimization for 2.5D Package Shock Impact Reliability", Huayan Wang[1], Jing Wang[1], Jiefeng Xu[1], Vanlai P ham[1], Seungbae Park[1,] Hohyung Lee[2], Gamal Refai-Ahmed[2] - [1]SUNY Binghamton, Binghamton, NY; [2]Xilinx Inc, San Jose, CA

2.5D packages have been widely used in the electronics industry for its high integration density and heterogeneous integration ability. It has become one of the best technical solutions for high-end products, such as GPU, computing, and FPGA. The package qualification process requires that it passes the board level drop test before shipping, however, this doesn't always guarantee that the package will survive from product level drop, especially for a complicated design product. It is critical to optimize the product design with consideration of package interconnections shock reliability.

In this study, the 2.5D package of a PCIe card's BGA failure risk in a drop event was analyzed both numerically and experimentally, and the product design was optimized. In the PCIe card, a 2.5D FPGA package was connected onto a PC board by the BGA. The heat sink was held onto the package with spring screws. The whole assembly was then sandwiched between two metal plates to improve the product integrity. Those parts can add large inertia to the package during the drop, which will pose more reliability risk on the BGA interconnections.

During the drop test, the PCIe card was inserted into a server box and fall together onto a drop table. The dye and pry result shows that the package experienced corner solder pad cratering failure. Finite element model of the PCIe card was built and validated by die surface stress measurement. The assembly initial warpage was taken into consideration during the die stress analysis. The direct acceleration method was used to simulate the product drop event. With the validated model, a parametric study was conducted regarding the top plate material, package edge bonding, SMD (solder mask design) and NSMD (none solder mask design)'s effect on the corner BGA stress level during the drop. The results show that the stainless-steel top plate can reduce the corner BGA stress compared with the aluminum top plate. The edge bonding can help to hold the package and PCB together during drop so that to reduce the corner BGA stress level. Compared with the NSMD case, the SMD can reduce the stress level of the corner BGA. The optimized design of the product shows a better drop reliability. This study provides a systematic way to analyze the 2.5D package product's BGA failure risk during a drop event and give guidance to optimize the product design.

"Testing and Evaluating Flexural Strength of Stacked Silicon Die Configurations", Ankita Korad[(1)], Daryl Santos[(1)], Krishnaswami Srihari[(1)], Salvatore Napoli[(2)] – [1]Watson Institute for Systems Excellence, SUNY Binghamton, Binghamton, NY; [2] Analog Devices, Inc., Wilmington, MA

Decrease in overall package size and package footprint coupled with increase in functionality and performance requirements, brings challenges of processing, handling, and assembling thinner dies in semiconductor packaging. At the same time, high reliability remains a critical necessity. In case of 3D packages or stacked die packages, structural integrity and mechanical robustness of the die stack is critical for its uncompromised functionality. In stacked die packages, silicon wafers must be backgrounded thinner, and dice are fixed by means of adhesive pastes or die attach films. Then the mechanical strength of the stacked structure is dominantly a function of the layers of die attach between multiple substrates and whether the package is a molded one or a cavity type. Due to its brittle nature, high flexural stresses induced in the die structure during packaging and assembly processes (thermomechanical stresses), and also during reliability and functionality tests, could result in detrimental fracture in the die. The purpose of this study is twofold:

- One is to develop an experimental test setup, select test variables and demonstrate good experimental setup repeatability and reproducibility for a simple 3-point flexural test to evaluate the flexural strength of stacked die configurations.
- Another is to identify, compare, and differentiate plausible stack attributes that contribute to varying flexural strength of stacked die configurations. The determined flexural load range and corresponding flexural extension at predefined failure mode (initial fracture in die) would be used to relatively compare these die configurations and comment on the packages' mechanical robustness. Data captured would help resolve future die failure problems encountered in new packaging and process development work.

"A High Spatial Resolution Measurement of Trap States and Charge Motion in Non-Traditional Semiconductors", Jason P. Moscatello[1], Christina L. McGahan[2], Katherine E. Aidala[3], [1]Researcher, Department of Physics, Mount Holyoke College[2]Post-doctoral Researcher, Department of Physics, Mount Holyoke College,[3]Chair of Physics, Professor of Physics, Chair of Engineering, Mount Holyoke College

Novel photovoltaics utilize non-traditional semiconductors (SC), with low mobilities compared to traditional SCs. Their transport is limited by trap states -- localized states which remove charge carriers from desired device processes -- which can dominate transport and evolve during continual operation.

Conventional measurements average over entire devices, providing no information on spatial variation. Scanning probe techniques offer a unique opportunity for high spatial resolution investigations of traps. Here we present a time-resolved Kelvin Probe Force Microscopy technique that enables recording local carrier motion and the ability to distinguish between populating and depopulating the trap states by studying materials in realistic device geometries.

"Liquid Metal Innovations for High-Performance TIMs", Timothy Jensen - Senior Product Manager

Solder Preforms & Thermal Technologies, Indium Corporation, Clinton, NY

The thermal conductivity values of metals make them highly sought after as a thermal interface material(TIM). In reality, the hardness of metals limits their effectiveness due to high interfacial resistance. There are a number of alloys that are liquid at or near room temperature. A liquid alloy is intriguing as you maintain the high thermal conductivity of metals, while mitigating the interfacial resistance issues that exist with solids. In this study, we explore methodologies and techniques that can enable liquid metal to be used in a wider array of TIM1 and TIM2 applications.

"Advances in Thermal Management", Brian Bruce, Mavyn Holman, & Paul Huynh – Epoxy Technology, Billerica, MA

High power density applications have created a need for new high thermal conductivity epoxy adhesives. Epoxy Technology has investigated the mechanism of thermal conductivity in silver filled electrically conductive epoxy adhesives. We utilized laser flash testing and SEM cross sections to determine how silver flake distribution effected thermal conductivity. We found cure, interface, and processing all play a significant role in an epoxy adhesives thermal conductivity and to better simulate in part resistance we propose a new laser flash sample preparation.

"Design of a Thermal Interface Material Cycling Reliability Test Program for Semiconductor Test", David L. Saums*, Principal - DS&A LLC, Amesbury MA; Tim Jensen, Sr. Product Manager - Indium Corporation, Clinton NY; Ron Hunadi, Market Development Manager - Indium Corporation, Clinton NY; Mohamad Abo Ras, CEO and Co-Founder - Berliner Nanotest und Design GmbH, Berlin, Germany

Requirements for semiconductor test and burn-in applications are very challenging for thermal interface materials (TIMs), including mechanical durability and temperature as well as thermal performance goals. A mechanical reliability test program has been developed and implemented for specialized TIMs developed specifically to meet those very challenging requirements for semiconductor test. Cycling with multiple contacts -- up to thousands of cycles with a single TIM -- is a long-sought development goal for the semiconductor test industry. These unusual industry requirements affect total cost, throughput, and yield for semiconductor test and achieving repeated, demonstrated high cycle counts is critical to cost reduction.

This presentation will describe an industry survey of requirements, development of a mechanical reliability test for evaluating durability, and test results for a family of specialized TIMs. The overall goal is to achieve 1,000 cycles in an automated system replicating the actual requirements found in high- volume semiconductor test; in addition to physical requirements, test data an evaluation for thermal resistance, thickness change, and visual analysis will be presented. All testing has been completed with an industry-standard, automated ASTM D5470-17 test stand that is commercially available.

"FTIR Based Identification Method of Underfill Materials and Matching System", Junbo Yang, Seungbae Park – SUNY Binghamton, Binghamton, NY

Epoxy-based underfill materials are used in microelectronic packaging to reduce coefficient of thermal expansion (CTE) between the organic substrate and the silicon device and thermal stresses on the solder joints. Using theorrect material properties of underfill materials can make fatigue life prediction using finite element method (FEA) more accurate. Therefore, identification method for cured underfill materials from assembly printed circuit board (PCB) is studied in this paper. Due to the tiny size, insoluble in organic solvent and hard to harvest, the Fourier-transform infrared spectroscopy microscope Attenuated total reflectance (FT-IR Microscope ATR) have been determined as the proper method to identify the underfill materials from assembly PCB. In this study, Using the Thermo-Nicolet 8700 with KBr beam splitters and ATR with Germanium crystal test specific underfill materials. Spectral combination method is used to exhibit peaks from each component of heterogeneous underfill mixture. Fingerprint region (from about 1500 to 500 cm^{-1}) which is due to all manner of bending vibrations within the molecule is the unique characterization for each underfill. Comparing the fingerprint region of each material, the peak value can effectively and efficiently identify different kinds of underfill. The underfill materials matching system program is also carried out based on the FTIR spectrum result.

"The Effect of Solder Paste Volume on Chip Resistor Solder Joint Fatigue Life", Huayan Wang, Ke Pan, Jonghwan Ha, Chongyang Cai, Jiefeng Xu, Seungbae Park – SUNY Binghamton, Binghamton, NY

The solder joint topology plays a significant role in determining its fatigue life. Due to the complex of the actual manufacturing environment, there are variations in solder volume for each joint. Which can induce the solder shape variations and misalignment of the chip resistor. The solder shape variation can severely affect its fatigue life. In this study, we use surface evolver software to calculate the solder shape with the global minimum energy. Finite element method was used to model the resistor solder joint under thermal cycling and to predict the fatigue life for different solder paste volume. Through varying the solder past volume to get different solder joint shape, the corresponding fatigue life was predicted. The result could provide a guideline for choosing optimal solder paste volume for surface mount components. Analysis results show that larger and balanced solder volume can give the best fatigue life under thermal cycling conditions.

Keywords: Self-alignment, Solder Paste Volume, Solder Shape, Fatigue Life.

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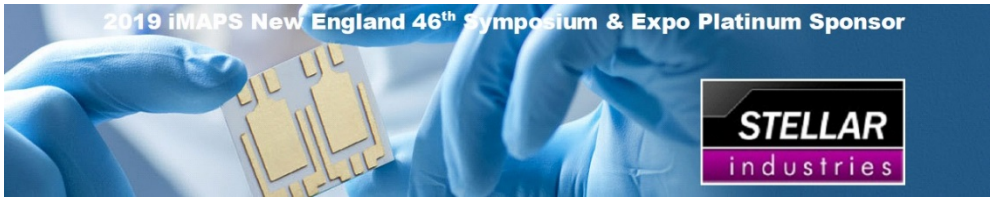

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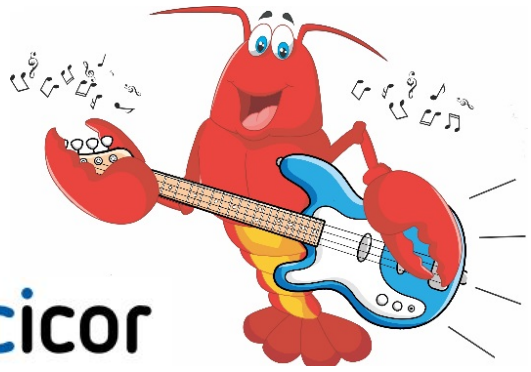

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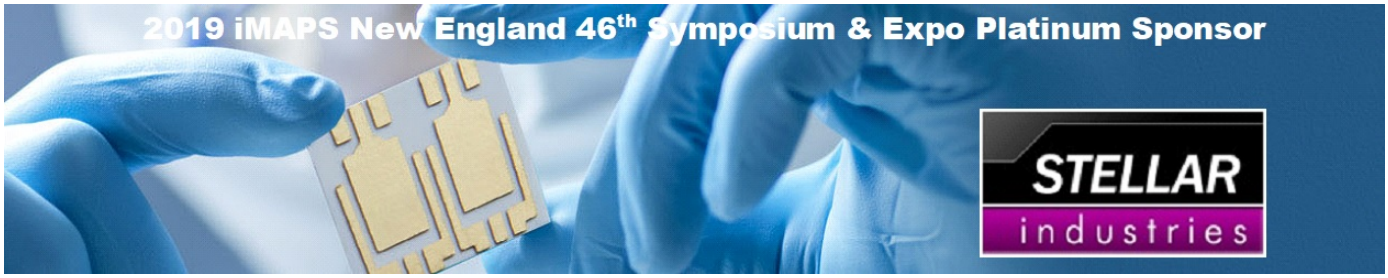

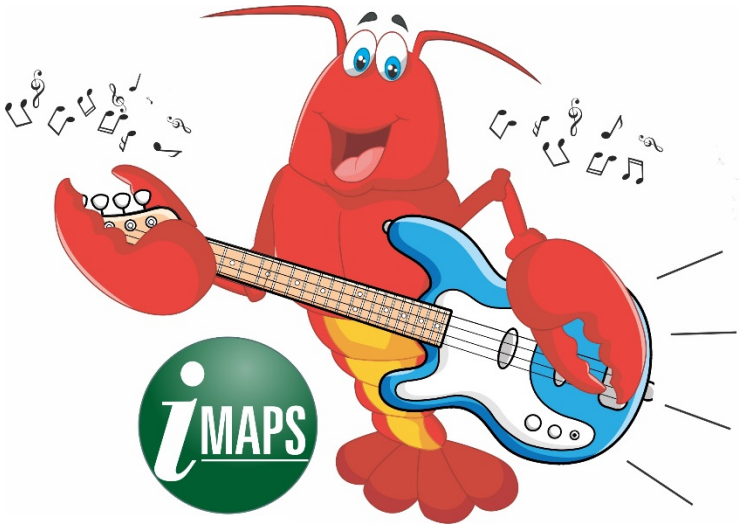

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